## REMARKS

### Status of the Claims

In the Office Action, claims 1-28 were noted as pending in the application. All claims stand rejected. To facilitate ease of examination and to focus examination resources on a preferred aspect, Applicant has combined the limitations of independent claim 11 with dependent claims 12, 13 and 14, and cancelled claim 11. Applicant has also cancelled claims 15-28 to streamline the examination process. Thus, pending independent claims 12-14 capture an aspect in a manner that shows they are not anticipated by or obvious over the cited references.

### A. Rejection of Claims 11-15, 17, 20-24 and 26 under 35 U.S.C. § 103(a).

On page 7 of the Office Action, claims 11-15, 17, 20-24 and 26 were rejected under 35 U.S.C. § 103 as being obvious over U.S. Patent Application Number US 2002/0088003 to Salee, ("Salee") in view of U.S. Patent Number 6,591,370 to Lovett, et. al. ("Lovett") in view of U.S. Patent Number 6,697,382 to Eatherton ("Eatherton"). The reasons that the pending claims patentably distinguish over the reference are addressed below.

### B. Summary of Cited References

Before addressing the Examiner's rejections, a brief summary of the cited references is provided.

#### Salee

Salee relates to a system for providing redundancy in a data over cable network that includes a plurality of CMTSs. ¶ 2. A timer preset register in a master CMTS stores a preset value and a comparator initiates a SyncPulse signal to slave CMTSs when a timer value equals the value stored in the preent register. ¶ 13. The timer preset value in every CMTS – including the master and all slaves - is set to the same value. ¶ 14 When the comparator of the master CMTS indicates a match between the preset register and the timer counter of the master, the SyncPulse signal then goes out to the slave CMTSs and instructs each salve to load the value from its respective preset register into its timer counter. *Id.*, ¶ 15, Claim 3. Thus, the timer counters of all CMTSs are synchronized at a frequency that is based on the value in the preset registers. ¶ 15. Changing the preset value P changes the time between SyncPulses being sent from the master to slave CMTSs. *Id.*

#### Lovette

Lovette relates to a computer system with distributed local clocks. One clock may be synchronized with another without affecting operation of the rest of the clocks in the system. Abstract. One clock is synchronized to another upon activation of a synchronization line, which is common to clocks being synchronized. FIG. 4 and col. 4, lines 44-62. Upon activation of the synchronization line, dynamic counters at the clocks reset. Id. Simultaneously with the resetting, the current output value of the reference clock is copied to a base register local to it. Id. This current output value of the reference clock is then copied to the base register of a clock being synchronized. Col. 4, lines 63-

65. Thus, the base registers of both the reference clock and the clock being synchronized have the same value. Since the output of each clock is the sum of the static value in its base register and the value of its dynamic clock, and the dynamic clocks were reset simultaneously, the outputs are the same.

**Eatherton**

Eatherton relates to distributing a global time value kept by a master component to other components of a packet switching system. Abstract. Each of various components determine a delay between it and another components sending it a global time update message. Id. "A master component periodically distributes a current global time to its neighbors, which in turn update their global time value and propagate the updated global time to their neighbors." Id.

**C. The Claims are not Obvious over the Cited References**

Applicant respectfully submits that the subject matter of the claims patentably distinguish over the cited references. Under MPEP § 2142, for an examiner to establish a *prima facie* case of obviousness, "three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure." If any of these three criteria are not met, the Examiner has not met the burden of establishing a *prima facie* case of obviousness, and the rejection should be withdrawn.

Furthermore, each dependent claim includes all of the limitations of the independent claim from which it depends. If an independent claim is non-obvious under 35 U.S.C. § 103, then any claim depending therefrom is non-obvious. MPEP §2143.03, citing In re Fine, 837 F.2d 1071 (Fed. Cir. 1988). Applicant respectfully submits that the burden of establishing a *prima facie* case of obviousness has not been met.

**D. Claims are not obvious over the cited references**

Since Examiner rejects the claims partially based on Salee and Lovett, Applicant repeats the analysis of Salee in view of Lovett for Examiner's convenience. Applicant provides analysis that addresses the new reference below following the heading NEW TEXT.

Regarding independent claims 11, 15, 20 and 24, a first value of a timing counter of a first circuit card is copied to a storage device, an offset is added to this value to create a future timing value that is then copied into the timing counter of a second circuit card. Claims 15 and 24 claim system hardware for facilitating the methods of claim 11 and 20. A timing value is written periodically from a system controller master to a circuit card slave. Page 14, lines 9-12. To obviate error caused by delay in writing the timing value from the master to the slave, a predetermined offset is added to the value of the master timing value before it is stored to the timing counter of the spare card. Page 14, lines 19-21. "The increased count value should be created such that the actual loading of

this increased count value into the slave timing counters (after distribution from the system Controller card to the cable interface cards) will occur exactly when the master timing counter on the system Controller card arrives at the value which is equal to the increased value." Page 15, lines 7-11. This provides the advantage that when a spare circuit card takes over for a failed circuit card, the timestamps are sent out from the newly-placed-into-service spare card in continuity with the timestamp stream that had been provided by the previous circuit card that the spare replaced. Page 15, lines 11-12.

This procedure is helpful when, for example, a circuit fails and a spare is automatically swapped into service as a replacement for the failed card. Or, when a card is physically replaced with a new card, and the new card takes over for a currently active card - a previously spare card, for example. In the latter case, the new card might have an empty timing counter register - capable of storing a timing value - because it has been out of service (i.e., on a shelf in a warehouse, for example), and would thus need a value placed into its timing counter. When a current timing counter value is distributed from the System Controller, by the time the value reaches the slave circuit cards, a finite amount of time will have passed, and the value will be stale, inasmuch as it represents a time that is not contemporaneous with the actual current time of the System Controller. By determining the amount of delay that occurs in distributing the timing value from the System Controller to the individual circuit cards, compensation is provided by adding this delay amount to the timing value from the System Controller, and then writing the sum to a given circuit card. Then, timestamps transmitted to the newly-placed-into-service card are time-continuous with the stream of timestamps that the previous card, which it replaces, had been transmitting.

This is distinguished from Salee in that the timing value in Salee is merely a predetermined value, representing a point in time, that occurs once every seven-minute (approximately) cycle. Par. 15. This value in Salee is an arbitrarily selected digital number placed into a register. Par. 13. This number is chosen to be a point in time from the set of points in time that will occur during a typical timing cycle, which the Salee applications states is approximately seven minutes. Thus, the arbitrary time P in Salee does not correspond to any jitter amount, delay amount, or time difference in bringing another device into service to replace a similar one that is taken out of service. It, the arbitrary time value P, is merely one of the plurality of incrementing time values that occur during a cycle, before the counters reset when another cycle begins. Basically, Salee teaches that active cards should be synchronized with one another at least once every timing cycle. This is also referred to in the first clause of the sentence of the present application that begins at page 13, lines 13-14, before the introduction of the claimed subject matter begins at page 13, line 16.

In contrast, the future timing counter value in the present application is a combination of the current timing value of the master timing controller value and an offset value. The offset value is chosen to equal the amount of time required to determine that a timing value needs to be inserted into a new card, and to actually update the new card's counter with the combined timing value. Thus, when the new card begins operating with the value that is transferred into it's timer, the same will be synchronized with the master system timing counter, which will have already advanced with respect to what it was when the determination was made that the new card needs to be pressed into service. Page 14, line 16 – page 15, line 12. Accordingly, the timing value P in Salee is

not the same as the future timing value as described and claimed in the present application.

With respect to Lovett, the reference does not teach copying a future timing value from one device to another to synchronize the clock of the other with the first device. Examiner states the Lovett discloses that a future timing value is copied from a first timing counter to a storage device local to a second circuit. Office Action ("OA") page 4, lines 1-2. Examiner also states that Lovett discloses copying a first timing counter value of the first circuit, or source, to a storage device local with respect to the second circuit, or node being synchronized, OA page 3, lines 17-19, implying that this is a claim element found in the reference. Applicant notes out that claim 11 does not recite "copying said first timing counter value into a storage device [] that is local with respect to the second circuit []." Furthermore, Applicant notes that claim 11 recites "copying said future timing counter value into the storage device that is local with respect to the second cable interface circuit." As Examiner stated, Salee does not disclose a future timing value.

Moreover, Lovett also does not disclose copying a future timing value. As discussed above, a future timing value is the sum of the reference, or first, timing value and a predetermined offset that corresponds to the time to copy a timing value from the first circuit to another circuit. When the future timing value has been calculated at the reference device, the future timing value is then copied to the device to be synchronized.

In contrast, Lovett clearly does not copy a future timing value. Lovett copies the timing value that is current when an activation of synchronization line 56, which is connected to both a source clock 19 and a clock to be synchronized 18. Col. 4, lines 63-65. After the copy process, both clocks 18 and 19 have the same value in their respective base registers. Thus, Lovett teaches copying a current timing value from base register 60 of source clock 19 to base register 52 of clock 18. Id. The value in dynamic counter 50 is added to the value in base register 52 after the value from base register 60 has been copied to base register 52. Therefore, the references do not disclose all of the elements recited in claim 11.

Furthermore, since the timing value copied from base register 60 to base register 52 is a current timing value (it's the value that is current when the synchronization line is activated), and the dynamic counter value is added thereto after the current value has been copied, Lovett teaches away from "copying said future timing counter value into the storage device that is local with respect to the second cable interface circuit."

In addition, combining Lovett with Salee does not result in a likelihood of success in arriving at the claimed subject matter. As discussed above, Salee teaches because slaving all CMTS devices to a master when a value in a preset register equals the value of a master timer. The present register in all CMTS devices contains the same value as all of the other preset registers. Thus, when the timer arrives at the present value, the master sends a sync pulse to all CMTS devices. Similarly, when synchronization line 56 is activated, as taught in Lovett, the current timing value from the source clock is copied from to its own base register as well as the base register of the clock being synchronized. Thus, devices in Salee all contain the same preset value in their registers and clocks in Lovett contain the same value in their base registers following activation of the synchronization line. However, claim 11 in the present application teaches that a value

stored at a reference circuit is different than the value copied into the storage device local to the circuit being synchronized. Therefore, following the teachings of the cited references would result in the same value being the storage devices local to each of the circuits, whether a reference circuit or a circuit to be synchronized. Since, the claim recites copying a future timing value rather than a current value, or a value that is the same as a value stored at the reference circuit, the method claimed in claim 11 cannot be performed by following the teachings of the cited reference.

Examiner agrees with Applicant's position given above. Page 4, lines 17-19. However, Examiner posits that although Lovett fails to disclose a future timing value being copied to a storage device local to the second cable interface circuit, Eatherton in combination with Lovett and Salee teach all of the elements recited in claim 11. Applicant disagrees with this position.

**NEW TEXT**

Examiner maintains the rejection based on the previous citations to Sallee in view of Lovett in view of newly cited Eatherton. Applicant believes that a brief refresher of the claimed technology will be helpful in light of the previous rejection and the new citation.

In particular, the present application discusses a fine-resolution synchronization of the timers at different nodes in the following excerpts. "If all the storage registers (503) on all cable interface cards are loaded with the same value and then all of the Trigger signals (502) to all of the cable interface cards are asserted at the same time, then all of the actual timing counters (512) will be loaded with the same value at the same point in time." Page 16, lines 2-5. As shown in FIG. 6, a system controller card (601) drives a Trigger that is sent to each cable interface card simultaneously. When each of the cable interface cards receives the Trigger signal, "then all of the actual timing counters (512) will be loaded with the same value at the same point in time. If the increased count value [is] calculated correctly, then the timing counter should not jump when the value is loaded into an already operating counter." Page 16, lines 5-6. Thus, when a spare circuit interface card takes the place of a failed interface card, there is no skip (either forward or backward) in the timestamp of packets sent from the card. This facilitates "[t]he difficult task [of ensuring during] the clock count/timer value distributions [] that the timing counters on all circuit cards load up the same value at substantially the same moment in time whenever a distribution occurs."

According to DOCSIS, two timestamps N1 and N2 transmitted successively at times T1 and T2 must satisfy the jitter requirement: $[(N2-N1)/10240000 - (T2-T1)] < 500$ nsec. To account for the loading of the timing counter value from a master timing counter to the timing counters of individual cards, an offset amount that equals the time to load the master timing count value into the timing controllers of each of the individual interface cards is added to the master timing count value and this future timing value is stored locally with respect to each of the cards. Page 14, lines 16-21. It will be appreciated that the value stored in the local register 503 of each of the interface cards is irrelevant as long as it is greater than the value of the master timing count value when the trigger signal is sent from the system control card. Indeed, in practice, the length of the physical wires, or traces, 502 are customized for each card location within a rack-mount chassis so that the time to traverse the wire 502 for each interface card is the same as for

the others. Furthermore, the lengths are designed so that the time to traverse the wires is the same as one cycle of the master clock of system control card 601 shown in FIG. 6. Thus, assuming a typical clock speed of 51.84 MHz MHz, one clock cycle equals 19.28 nsec, which is the degree of accuracy the claimed subject matter of an aspect can synchronize cable interface cards with one another, and to a system controller.

The DOCSIS specification that the timer values in the two nodes should be synchronized to within 500 nsec is much more demanding than the requirements in Eatherton. Indeed, the techniques described in the Eatherton patent could never provide a level of synchronization with 500 nsec accuracy because it describes "[a] goal of certain embodiments is to align the time counters of all components within a packet switching system within some small time variance, such as a few packet times or some small time variance. Col. 4, lines 27-30. As one skilled in the art would appreciate, the maximum size of an IP packet is 65,535 bytes and even a typical Ethernet packet size is 1,500 bytes, which is 12,000 bits. Assuming a conservative 10 GHz clock speed for Ethernet (typical speeds currently may be 1 GHz) a typical Ethernet packet would take 1.2 μS "a few [] times", which is clearly more than 500 nS, as well as the accuracy achievable following the claimed subject matter.

The reason the times discussed in Eatherton are much larger than the small amounts achieved by the claimed subject matter is that in Eatherton, the times being synchronized relate to packet's time stamps and not system clock synchronicity times. In Eatherton, actual values of time are represented in the message being sent and received by various components. Col. 4, lines 15-25. Furthermore, the step of distributing a time value may be repeated to determine the current delay time used in transmitting the message. Packets may be sent back a forth several times to determine an update delay amount. Col. 4, lines 63-66. As shown in FIG. 3 of Eatherton, a packet is sent with its departure time determined by the local clock of the sending device, and then the arrival time is inserted at the receiving device based on its internal clock counter. From this the update delay is calculated at step 368. Thus, regardless of the timer count value of the sending and receiving devices, the difference between them is calculated and used for the update delay. It will be appreciated that one skilled in the art would apply the discussions in Eatherton to the synchronization between network devices, such as for example, switches, networks, computers or combinations thereof as listed in Eatherton at col 1, lines 31-34, such components being known to be manufactured by the assignee of Eatherton, or Cisco Technologies, Inc. Typically these devices are separated by miles of cable and achieving synchronization between corresponding system clocks of "a few packet times" is sufficient for the purposes for which Eatherton applies.

In stark contrast, however, in the present application actual delay times are not calculated and then transmitted to various interface cards. As claimed in amended claim 12, a future timing value is copied into a register local to a card to be synchronized and then after waiting a predetermined amount of time the future timing value is copied into the timing counter of the card to be synchronized, the predetermine amount of time elapsing when the timing counter value in the synchronizing timing counter (the first interface card as claimed in claim 13, for example) is substantially equal to the timing counter value of the card to be synchronized (the second interface card as claimed in the claim). It will be appreciated that the determination of the future timing value as claimed in claim 13 is but only one embodiment of determining a future timing value. Typically,

the scenario addressed by claims 12, 13 or 14 would be where the first card is a failing or failed card and the second card is a spare being switched to begin serving the load that was previously served by the first card. However, it will be appreciated that typically a trigger signal is sent to all interface cards at the same time and they all load the same future timing value into their respective timing counter at the same time. Basically what is the claims are claiming is generating a future timing value that is greater than the current time of the current timing value of the master control card and sending that value to all of the interface cards. When the system control timing counter value equals one cycle less than the future timing value (i.e., the leading edge of the clock cycle that has a value one less than the future timing value, for example) a Trigger signal is sent to all interface cards via a physical line. As discussed above, the length of the line is designed so that when the Trigger signal triggers all of the interface cards to load the future timing value into their respective counters, the leading edge of the clock signal cycle that equals the future timing value will simultaneously rise to its high level. Thus, the system controller clock and the interface cards all have the same value in their timing counter.

The need for the exceptional accuracy, with respect to the level of accuracy referred to in Eatherton, provided the motivation to add the point-to-point Trigger signals shown in FIGS. 5 and 6. These Trigger signals are the key to making the idea work. Without the Trigger signal being delivered to each of the individual cards simultaneously, so that that the timing counter of each of the interface cards would equal the value of the system control card timing counter, 500 nsec accuracy could not be obtained. Eatherton does not disclose these Trigger signals.

Eatherton focuses on a technique whereby one node determines the fixed, but unknown update delay (a measurement of the difference in timer values plus the transmission delays between different nodes), and then it distributes a new timer value to the second node to correct its clock. As discussed above, the Eatherton approach cannot provide the type of fine-grain timer synchronization that is claimed in the claims of the present application. Thus, not only are all of the elements of the claims of the present application not included in the references, either alone or in combination, there is not a likelihood of success in combining the references, because flowing the teachings of Eatherton would result in much larger inaccuracy in synchronization of the interface cards.

Furthermore, there is not a teaching, suggestion or motivation to combine the references because Eatherton relates to synchronizing components that may be separated by many miles and also because Eatherton teaches calculating a delay time and then adding that to the actual clock value of a synchronizing component after it propagates to the component to be synchronized. This starkly contrasts with triggering multiple interface card registers to load a future timing value into respective timing counters when a system controller timing counter equals the future timing counter value. Therefore, examiner has not made out a *prima facie* case of obviousness.

Accordingly, Applicant respectfully requests withdrawal of the rejection of pending independent claims 12-14.

**SUMMARY**

For all the reasons advanced above, Applicant respectfully submits that the application is in condition for allowance and that action is earnestly solicited.

If the Examiner believes that there are any issues that can be resolved by a telephone conference, or that there are any informalities that can be corrected by an Examiner's amendment please contact the undersigned at the mailing address, telephone, facsimile number, or e-mail address indicated below.

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